REMARKS/ARGUMENT

Claims 1-21 are pending in the application. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Eikemeyer (U.S. Patent No. 6,694,425) ("Eikemeyer"). Claims 1, 10 and 16 are amended.

Applicants respectfully submit that the cited references do not teach, suggest or disclose "[a] method comprising: ... flushing an instruction from said first thread from a pipeline of said processing system after a predetermined number of clock cycles if data is to be loaded from said memory device before executing said instruction" (e.g., as described in claim 1).

The Office Action asserts that Eikemeyer teaches the relevant limitations at column 13, lines 5-15 and column 5, lines 26-30. *See* Office Action dated 12/21/2005, paragraph 7. Applicants disagree.

Column 13, lines 5-15 state:

> After a thread has been dispatch-flushed and is restored, it reenters the pipeline as normal. Should it again encounter the dispatch block or a different block, the dispatch flush can occur again. A dispatch block caused by a sync instruction, an L2 cache miss, or other long latency event for a thread may last a long time so the restart of the stalled thread could be delayed, thereby giving more cycles to the other threads. In any event, it may be preferable to refrain from fetching or decoding the stalled thread again at the thread select locations 280a, 280b until, e.g., the stalled condition resolves itself or until a predetermined number of machine cycles has passed.

First, Applicants note the present reference is directed toward what can be done with a thread *after* it has been flushed. The relevant limitation of claim 1 discussed above is directed toward an instruction *before and during* a flush.

In particular, the cited section discusses a *previously flushed* instruction may reenter the pipeline normally, or it may be flushed again. If the instruction is flushed

again (because of a cache miss or a latency event), it may be preferable to *delay the reentry* to allow for more cycles for other threads. It further states it may be preferable to wait to fetch or decode the stalled thread until a predetermined number of machine cycles have passed. However, waiting to fetch or decode the stalled thread until a predetermined number of machine cycles have passed is not the same as flushing an instruction from said memory device after a predetermined number of clock cycles if data is to be loaded from said memory device before executing said instruction as described in embodiments of the present application. Applicants submit the cited section fails to teach or suggest the relevant limitations.

Column 5, lines 23-30 (including the cited lines 26-30) state:

> The method may also comprise restarting the thread whose instructions were flushed from the dispatch stages and all stages in the processor pipeline prior to the dispatch stage. The step of restarting may be delayed until a condition which causes the stalled instruction to stall at the dispatch stage is resolved. The step of restarting the flushed thread may also be delayed until a number of the processor cycles have passed.

The cited section discusses restarting a *previously flushed* thread. The reentry may be delayed until a condition causing the stall is resolved or until a number of processor cycles have passed. Again, similar to the cited section discussed above, Applicants submit this cited section is directed toward what can be done with a thread *after* it has been flushed, while the relevant limitation of claim 1 discussed above is directed toward an instruction *before and during* a flush. Delaying the restart of a previously flushed thread for a number of processor cycles is not the same as flushing an instruction from said memory device after a predetermined number of clock cycles if data is to be loaded from said memory device before executing said instruction as described in

embodiments of the present application. Applicants submit this cited section fails to teach or suggest the relevant limitations as well.

Therefore, since each and every limitations is not found in the cited reference, the cited reference cannot adequately form the basis of a proper 35 U.S.C. §102(e) rejection of independent claim 1. Independent claims 5, 10, and 16 contain substantively similar limitations and therefore are also allowable for similar reasons. Claims 2-4, 6-9, 11-15 and 17-21 depend from allowable independent claims 1, 5, 10 and 16, and therefore are in condition for allowance as well.

For at least the above reasons, Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON LLP

Date: January 2, 2007

By: _____
Sumit Bhattacharya
(Reg. No. 51,469)

KENYON & KENYON LLP
333 West San Carlos St., Suite 600
San Jose, CA 95110
Telephone: (408) 975-7500
Facsimile: (408) 975-7501

95756